By virtue of the regions K1 and K2, there is also an improvement in the mobility of electrons. In case of FIG. 7B according to the prior art, the doping profile of p type impurity ions is totally uniform in the channel region. Consequently, the possibility of an occurrence of bulk punch through becomes high. Furthermore, the mobility of electrons is reduced.

In case of FIG. 8A according to the present invention, the doping concentration of p type impurity ions exhibits a peak value at a region located beneath the center portion of channel region. Accordingly, an occurrence of bulk punch through is avoided. In case of FIG. 8B according to the prior art, the doping profile of p type impurity ions is totally uniform in the channel region. Consequently, the possibility of an occurrence of bulk punch through becomes high.

FIG. 9A shows a potential contour taken along the line a—a' in FIG. 4M according to the present invention, whereas FIG. 9B shows a potential contour taken along the line c—c' in FIG. 1C according to the prior art.

Referring to FIG. 9A, it can be found that the channel region located beneath the gate exhibits high potential and that the width W1 of a depletion region is relatively wide. On the other hand, in case of FIG. 9B, the channel region located beneath the gate exhibits lower potential than that of FIG. 9A. Also, the width W2 of a depletion region is narrower than the width W1 of FIG. 9A.

On the other hand, the junction capacitance C between the n type source/drain regions and the p type silicon substrate is inversely proportional to the square root of the width W of depletion region, as expressed by the following equation (1):

$$C \propto \frac{1}{\sqrt{W}} \quad (1)$$

Therefore, the structure of the present invention exhibits a relatively low junction capacitance, as compared with the prior art.

In the channel region, current flows generally along the surface of the substrate. FIG. 10A shows the amount of current I_D varying depending on the variation in the gate voltage V_G, in case of the structure of FIG. 1C according to the prior art. Referring to FIGS. 10A and 10B, it can be found that upon the variation in the gate voltage V_G, the case shown in FIG. 10A exhibits a larger amount of current flow than that of FIG. 10B. Accordingly, the structure of the present invention has a superior electron mobility characteristic, as compared with the prior art.

As apparent from the above description, the present invention provides a MOSFET with a LDD structure wherein the doping concentration of channel ions exhibits a peak value at opposite edges of a gate and a substrate bulk located beneath a channel region With this structure, it is possible to avoid an occurrence of bulk punch through, reduce the junction capacitance and enhance the electron mobility.

Although the preferred embodiments of the invention have been disclosed for illustrative purpose, those skilled in the art will appreciated that various modifications, additions and substitutions are possible, without departing from the scope and spirit of the invention as disclosed in the accompanying claims.

What is claimed is:

1. A method of making a metal oxide semiconductor field effect transistor comprising the steps of:

defining an active region and a field region in a substrate of a first conductivity type by forming a field oxide film over the field region;

forming a first insulation film and a second insulation film, in this order, on the entire regions of said substrate;

patterning said second insulation film located in said active region to remove a portion of said second insulation film corresponding to a gate region and thus expose a portion of said first insulation film through said removed portion of the second insulation film;

patterning said exposed portion of the first insulation film to remove its part having a width narrower than the width of said gate region and thus leave a part of the first insulation film having a predetermined width not covered with the second insulation film;

implanting a channel impurity of the first conductivity type at a predetermined concentration in regions located beneath surface portions of the substrate corresponding to opposite edges of the gate region and in the bulk substrate below the center portion of a channel region, using the remaining second insulation film located beyond the gate region, as a mask;

forming a pair of first impurity regions at said regions located beneath said substrate surface portions corresponding to opposite edges of the gate region, respectively, and a second impurity region in said bulk substrate in a location corresponding to said center portion of the channel region;

removing a portion of the first insulation film remaining at the opposite edges of the gate region;

forming a gate at a region shaped into a concave shape by the removal of first and second insulation films;

removing all portions of the first and second insulation films remaining beyond the gate region;

implanting a low concentration impurity of a second conductivity type using said gate as a mask, to form low concentration source and drain regions in the substrate;

forming side wall insulation films at opposite side surfaces of the gate; and

implanting a high concentration impurity of a second conductivity type using the gate and said side wall insulation films as a mask, to form high concentration source and drain regions in the substrate.

2. A method of making a metal oxide semiconductor field effect transistor in accordance with claim 1, wherein a pad insulation film is formed prior to said step of forming said first insulation film and removed along with the first insulation film at said step of removing the first insulation film carried out after the implantation of said channel impurity of the first conductivity type in the substrate.

3. A method of making a metal oxide semiconductor field effect transistor in accordance with claim 1, wherein said step of leaving a part of the first insulation film having a predetermined width not covered with the second insulation film comprises the steps of:

forming a third insulation film over the entire exposed surface after the formation of said concave region formed by the removal of the second insulation film from the gate region, said third insulation